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APPLICATION NO.	FI	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/622,937	10/622,937 07/18/2003		Karl Schrodinger	M&N-IT-462	M&N-IT-462 3471	
24131	7590	07/29/2004		EXAMINER		
LERNER A	ND GRE	EENBERG, PA	NGUYEN, HAI L			
P O BOX 248	30					
HOLLYWOOD, FL 33022-2480				ART UNIT	PAPER NUMBER	
•				2816		

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	K				
	Office Action Commence	10/622,937	SCHRODINGER, KARL	بر. -				
	Office Action Summary	Examiner	Art Unit					
		Hai L. Nguyen	2816					
	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status								
1)🛛	Responsive to communication(s) filed on <u>04</u>	November 2003.						
2a) <u></u> □	This action is FINAL . 2b)⊠ Th	is action is non-final.	•					
3) 🗌	☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D. 11, 4	53 O.G. 213.					
Disposition of Claims								
4) 🖂	Claim(s) 1-21 is/are pending in the application	n.						
	4a) Of the above claim(s) is/are withdrawn from consideration.							
5) 🗌)☐ Claim(s) is/are allowed.							
6)⊠	Claim(s) <u>1-21</u> is/are rejected.							
	Claim(s) is/are objected to.							
8)[_]	Claim(s) are subject to restriction and	or election requirement.						
Applicati	on Papers							
9)	The specification is objected to by the Exami	ner.						
10)⊠ The drawing(s) filed on <u>04 November 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
_	Replacement drawing sheet(s) including the corre	• • • • • • • • • • • • • • • • • • • •	•					
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority u	ınder 35 U.S.C. § 119							
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).								
a)⊠⁻All─b)⊡⁻Some⁻*⁻c)⊡⁻None⁻of:								
1. Certified copies of the priority documents have been received.								
2. Certified copies of the priority documents have been received in Application No								
3. Copies of the certified copies of the priority documents have been received in this National Stage								
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.								
	oo the attached detailed Office action for a li	st of the confined copies not receive	M.					
Attachment	(c)							
	e of References Cited (PTO-892)	4) Interview Summary	(PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date								
	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/0 · No(s)/Mail Date <u>7/18/03</u> .	8) 5) ☐ Notice of Informal P 6) ☐ Other:	ratent Application (PTO-152)					
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DETAILED ACTION

Claim Rejections - 35 USC § 112

- 1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 2. Claims 1-9 and 11-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is indefinite because the limitation "an offset compensation circuit connected to the first and the second inverters and adjusting a difference between the two output clock signals to a constant value", in the last 3 lines, is misdescriptive. The specification (page 19, line 11 through page 20, line 3) clearly discloses that the offset compensation circuit (8 in instant Fig. 2) is connected to the differential amplifier (3 in instant Fig. 2) for providing a control voltage (Vcmc in instant Fig. 5) to the differential amplifier, which will then output the voltage signals (Dp, Dn) being superposed by an offset voltage. As a result, the voltage signals (Dp, Dn) is adjusted to the optimum switching point of the respective inverters so an optimum output pulse shape of the output clock signal can be achieved such as "a difference between the two output clock signals to a constant value". Therefore, the offset compensation circuit connected to the differential amplifier for adjusting the output voltage signals of the differential amplifier in order to achieve the result as "a difference between the two output clock signals to a constant value" rather than connected to the first and the second inverters and adjusting a difference between the two output clock signals to a constant value.

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Claim 4 is indefinite because of the limitation "a further differential amplifier generating first and second amplified", in lines 6-7, is unclear. Insofar as understood, the recited limitation "an input differential amplifier generating first and second amplified signals in response to first and second differential input clock signals; first and second inverters connected to the input differential amplifier and generating respective first and second differential output clock signals", as recited in base claim 1, refers to (the amplifier 3, inverters In1 & In2 in instant Fig. 2). Therefore, it is not clear how the above limitation reads on the preferred embodiment.

Claims 2, 3, 5-9, and 12-21 are rejected due to their dependencies on the base claims 1 and 4.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: a differential amplifier (2 in instant Fig. 2) and an integrator (7). In order for the control circuit (2, 3, 4, 5, 7, 8 in instant Fig. 2) for driving the inverters (In1, In2) and shifting the input pulses of the inverters to the optimum switching point of the inverters, those omitted elements need to be included in the claim (see the specification; page 5, line 18 through page 6, line 24).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

⁽b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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4. Claims 1-3 and 21, to the extent understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (US 6,081,162).

With regard to claim 1, Johnson discloses in Figs. 1-3 a circuit configuration for regenerating clock signals (115A, 115B), comprising: an input differential amplifier (108) generating first and second amplified signals in response to first and second differential input clock signals (103A, 103B); first and second inverters (112A, 112B) connected to the input differential amplifier and generating respective first and second differential output clock signals (115A, 115B); and an offset compensation circuit (116).

With regard to claims 2-3 and 21, the references also meet the recited limitations in these claims.

5. Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Johnson.

With regard to claim 10, Johnson discloses in Figs. 1-3 a circuit configuration for regenerating clock signals (115A, 115B), comprising: an input differential amplifier (108) generating first and second amplified signals in response to first and second differential input clock signals (103A, 103B), first and second inverters (112A, 112B) connected to the input differential amplifier and generating respective first and second differential output clock signals (115A, 115B) from the first and second amplified signals, the inverters having respective input pulse shapes and an optimum switching point (see column 2, line 26 through column 4, line 16), and a control circuit (116) for driving the inverters and shifting the input pulses of the inverters to the optimum switching point of the inverters.

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Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Rodgers et al. (US 6,362,737).

The above-discussed circuit of Johnson meets all of the claimed limitations except for the limitation that the differential output clock signals are fed to a differential line driver.

Rodgers et al. teaches in Figs. 24-29 a circuit having antenna bus 132 that uses differential line drivers for all differential signals as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize differential line drivers taught by Rodgers et al. in Figs. 1-3 of Johnson for the advantage of distributing over a long-distance wire communication with an improved noise immunity characteristic.

Conclusion

- 8. Regarding claim 11, the patentability thereof cannot be determined because of the claim as being incomplete for omitting essential elements.
- 9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Hu (US 6,633,191) is cited as of interest because it discloses a clock buffer with DC offset suppression circuit.

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10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN #10 July 16, 2004

TMMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800